



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/US00/05545 (22) International Filing Date: 01 March 2000 (01.03.2000) (30) Priority Data: 60/122,217 01 March 1999 (01.03.1999) US (60) Parent Application or Grant PHOTOBIT CORPORATION [/]; O. FOSSUM, Eric [/]; O. BEREZIN, Vladimir [/]; O. FOSSUM, Eric [/]; O. BEREZIN, Vladimir [/]; O. HARRIS, Scott, C. ; O.	Published	
(54) Title: ACTIVE PIXEL SENSOR WITH FULLY-DEPLETED BURIED PHOTORECEPTOR (54) Titre: DETECTEUR DE PIXELS ACTIFS A PHOTORECEPTEUR ENTERRE A DEPLETION COMPLETE (57) Abstract <p>A fully depleted photodiode (200) accumulates charge into both the photodiode (200) and a separate floating diffusion (205). The photodiode (200) is a buried photodiode having two PN junctions for photocarrier conversion. The floating diffusion (205) has less capacitance than the overall photodiode, thereby resulting in a knee-shaped transfer characteristic for charge accumulation that results in a larger dynamic range. The floating diffusion (205) is connected to an output transistor (210). A reset transistor has a gate (206) that is activated to connect the floating diffusion (205) to a diffusion region (208) that is held at VDD to reset the photodiode (200).</p> (57) Abrégé <p>Une photodiode (200) à déplétion complète accumule une charge à la fois dans ladite photodiode (200) et dans une région de diffusion flottante séparée (205). La photodiode (200) de type enterré possède deux jonctions PN qui permettent la conversion d'un photoporteur. La région de diffusion flottante (205) présente une capacitance inférieure à celle de la photodiode globale, ce qui produit une caractéristique de transfert en forme de genou permettant d'accumuler une charge qui produit une plage dynamique plus grande. La région de diffusion flottante (205) est connectée à un transistor de sortie (210). Un transistor de remise à l'état initial possède une grille (206) qui est activée afin de connecter la région de diffusion flottante (205) à une zone de diffusion (208) qui est maintenue au niveau de VDD, afin de remettre la photodiode (200) à l'état initial.</p>		



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<p>(21) International Application Number: PCT/US00/05545</p> <p>(22) International Filing Date: 1 March 2000 (01.03.00)</p> <p>(30) Priority Data: 60/122,217 1 March 1999 (01.03.99) US</p> <p>(63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application <div style="display: flex; justify-content: space-between;"> US Not furnished (CON) </div> <div style="display: flex; justify-content: space-between;"> Filed on Not furnished </div> </p> <p>(71) Applicant (for all designated States except US): PHOTOBIT CORPORATION [US/US]; 7th floor, 135 North Robles Avenue, Pasadena, CA 91101 (US).</p> <p>(72) Inventors; and</p> <p>(75) Inventors/Applicants (for US only): FOSSUM, Eric [US/US]; Photobit Corporation, 135 North Los Robles Avenue, 7th floor, Pasadena, CA 91101 (US). BEREZIN, Vladimir [US/US]; Photobit Corporation, 135 North Los Robles Avenue, 7th floor, Pasadena, CA 91101 (US).</p>		<p>(74) Agent: HARRIS, Scott, C.; Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA 92122-1243 (US).</p> <p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report.</i></p>
<p>(54) Title: ACTIVE PIXEL SENSOR WITH FULLY-DEPLETED BURIED PHOTORECEPTOR</p>		
<p>(57) Abstract</p> <p>A fully depleted photodiode (200) accumulates charge into both the photodiode (200) and a separate floating diffusion (205). The photodiode (200) is a buried photodiode having two PN junctions for photocarrier conversion. The floating diffusion (205) has less capacitance than the overall photodiode, thereby resulting in a knee-shaped transfer characteristic for charge accumulation that results in a larger dynamic range. The floating diffusion (205) is connected to an output transistor (210). A reset transistor has a gate (206) that is activated to connect the floating diffusion (205) to a diffusion region (208) that is held at VDD to reset the photodiode (200).</p>		

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Description

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ACTIVE PIXEL SENSOR WITH FULLY-DEPLETED BURIED
PHOTORECEPTOR

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefit of U.S. Provisional application No. 60/122,217, filed March 1, 1999.

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BACKGROUND

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Active pixel sensors are well known in the art. The basic active pixel sensor is described in U.S. Patent No. 5,471,515.

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Active pixel sensors can use different kinds of active elements as their charge receiving elements. FIGS. 1A - 1C show three different examples of three of the common image sensing active elements.

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A basic photodiode active pixel is shown in FIG. 1A. This includes a photodiode 100 on the substrate below an active oxide 102. The photodiode is connected directly to an output transistor 104. A gate 106 connects the photodiode 100 to a diffusion region 108 that is held at a voltage VDD.

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The photodiode can be reset by activating gate 106, connecting the photodiode to VDD. Subsequent accumulation of charge changes the voltage on the photodiode.

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5 The basic photogate active pixel sensor is shown in
FIG. 1B. The active photogate 120 connects to the output
10 transistor 122 through a transfer gate 124. This
facilitates correlated double sampling in which the level
of the photogate is first tested, then charge is
15 transferred, and the value obtained again. Only the
difference between the two charge amounts are used as an
indication of the output. Hence, the output better
20 indicates the amount of photogenerated electrons.

FIG. 1C shows the so-called pinned photodiode being
25 used as an active element in an active pixel sensor. The
pinned photodiode is shown in U.S. Patent No. 5,625,210.
A transfer gate with channel implant 140 is used to
30 transfer the charge out of the photodiode 142. The
channel implant is used to adjust the bias of the pinned
photodiode to facilitate charge output.

SUMMARY

40 The present system teaches using a fully-depleted
buried photoreceptor with a coupled floating diffusion.
The photoreceptor can be a "buried" diode, with an
45 overlying portion of substrate.

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BRIEF DESCRIPTION OF THE DRAWINGS

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These and other aspects will be described in detail with reference to the accompanying drawings, wherein:

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FIGS. 1A - 1C show prior photosensitive elements as used in active pixel sensors;

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FIG. 2A shows a photosensor of an embodiment in which the output transistor is directly connected to the photosensor;

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FIGS. 2B - 2D show potential level diagrams for such a device;

30

FIG. 3 shows an alternative system in which a transfer gate is used to support correlated double sampling

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FIG. 4 shows a fabrication layout of the system using a P-type buried photosensor with an N-well and a P-well; and

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

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An embodiment uses a fully depleted buried photodiode 200 as the photosensitive element. This photodiode is connected to a floating diffusion 205. That diffusion forms the output, either directly or via a transfer gate. The floating diffusion 205 is connected

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5 to an output transistor 210, e.g. a transistor that is
configured as a source follower. A reset transistor 205
10 has a gate 206 that is activated to connect floating
diffusion to a diffusion region 208 that is held at VDD.
This resets photodiode 200. The floating diffusion with
15 reset transistor forms a vertical diffusion shield 600
located between the depleted photodiode 200 and the
diffusion region 208. This is shown in Figure 2B.

20 The buried photodiode has two PN junctions for
photocurrent conversion. Assuming that the buried
photodiode 200 is of N-type, there is a first PN junction
25 between the P-type substrate material 212 above the
photodiode and the N-type photodiode itself. A second PN
30 junction exists between the N-type photodiode 200 and the
underlying P-type material 214. The two PN junctions
have different photosensitivities in specific spectral
35 ranges. For example, the upper PN junction near 212 may
increase the photosensitivity to blue and green. The
lower PN junction may increase the photosensitivity to
40 green and red. These surface components can constitute
one of the largest sources of leakage current for PN
45 junction technologies. In addition, the dark current can
be reduced by eliminating certain surface components.

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5 The two different embodiments are optimized for
different applications. The first embodiment is shown in
10 Figure 2A. A silicon substrate 199 has a buried, fully
depleted photodiode 200 formed therein. For purposes of
this illustration, the photodiode will be assumed to be
15 of N-type, in a P-type substrate. A layer of P material
212 overlies the top surface 216 of the photodiode, and
the P-type material 199 surrounds all sides of the fully
20 depleted photodiode.

 The upper surface of the silicon includes an active
25 oxide region 220, and a field oxide region 222. A space
224 is left between the edges of the photodiode 200 and
the field oxide 222. This space 224 has been found to
30 avoid mechanical stresses from the field oxide.

 In the Figure 2 embodiment, the floating diffusion
region 205 is connected directly to the photodiode 200.
35 This floating diffusion region 205 can have the same
impurity as the buried photodiode but at a higher
concentration. The floating diffusion 205 is also
40 connected to the output transistor 210. In addition, the
floating diffusion is connected through a surface gate
206 to a diffusion region 208 that is biased at VDD.
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 Operation is shown in Figures 2B and 2C. Actuating
the reset gate 206 brings the floating diffusion 205 to
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5 VDD, thereby lowering the vertical diffusion shield 600,
and allowing any charge in the photodiode (shown as 602)
10 to dump into the diffusion region 604. Turning off the
reset transistor 206 again raises the vertical diffusion
bridge 600, and thereby again causes the charge to
15 accumulate.

The charge accumulation occurs in two different
stages which produces effectively a knee-shaped response
20 slope. The slope of Voltage out as a function of
incoming light is shown in Figure 2D. The first slope
610 occurs during the first part of the signal
25 accumulation. During the part, the charge can accumulate
in a relatively small "bucket", shown as portion 606.
30 This small bucket represents the floating diffusion.
This relatively small bucket has low capacitance, and
hence can accumulate the charge particles quickly. This
35 charge accumulates in the small bucket, according to a
first response slope shown as the first slope portion
610.
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Once the small bucket portion is filled (effectively
the floating diffusion 205 is filled with charge), then
45 charge begins accumulating in the higher-potential buried
diode portion 200. This charge accumulation is held in a
larger bucket. The accumulation in the larger bucket is
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5 shown as 614. The operation produces a voltage-to-light transfer characteristics of a second slope 612.

10 The knee-shaped accumulation can be used for certain advantageous operations. A reason for obtaining the knee-shaped accumulation in this embodiment, however, is to compress the higher light portion, and accentuate the
15 lower light portion. This enables the system to therefore obtain a larger dynamic range.

20 A second embodiment is shown in Figure 3. In this embodiment, a separate floating diffusion 305 is in contact with the buried fully depleted photodiode 200. A
25 separate input transistor 308 separates between the floating diffusion 305 and the output floating diffusion 205 connected to output transistor 210. The output floating diffusion 205 is also connected to the diffusion region in a similar way to that described above in the
30 Figure 2 embodiment. The input transistor 308 can be used to separate the two processes of photocharge integration and signal charge readout to facilitate
35 correlated double sampling in order to reduce the KTC noise and parallel shutter. Like in the first embodiment, this system uses a controllable vertical
40 diffusion bridge 305 to control the charge from the fully depleted photodiode. This system also leaves a space 224
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5 between the top surface of the photodiode and the silicon
substrate, thereby providing the same material as the
10 silicon substrate above the photodiode as below the
photodiode.

15 Implementation is shown in Figures 4 and 5, which
show the wells that are used and the masks used to form
those wells. Figure 4 shows a deep buried photodiode
using an N-well. In this embodiment, the photodiode is
20 buried more deeply. Figure 5 shows a shallow buried
photodiode using a P-well. As discussed above, the
shallow and deep burying at the wells can be used for
25 different purposes.

Correlated double sampling occurs as follows.
30 First, the whole system is reset by turning on the reset
transistor gate 206 at the same time that the input
transistor gate 310 is activated. This has the effect of
35 resetting the floating diffusion 205, the second floating
diffusion 305, and the buried fully depleted photodiode
200. After that, the gate 206 is turned off to raise the
40 vertical diffusion bridge. At that time, the output
transistor 210 is used to sample the value on floating
diffusion 205. This represents the reset level. The
45 output transistor 308 is then turned off, and charge is
allowed to accumulate. At the end of the charge
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5 accumulation, the output transistor 308 is turned back
on, allowing the output transistor 210 to sample the
10 value of charge stored in the photodiode.

This system enables increasing the quantum
efficiency or spatial resolution. Since the spatial
15 resolution is proportional to the pixel size, this system
could obtain an increased internal gain.

Although only a few embodiments have been described
20 in detail above, other embodiments are contemplated by
the inventor and are intended to be encompassed within
the following claims. In addition, other modifications
25 are contemplated and are also intended to be covered.

Claims

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What is claimed is:

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1. A photosensor comprising:

a semiconductor substrate;

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a buried photodiode in said semiconductor substrate,
having a top surface which is separated from a surface of
the substrate by a first area of the substrate, and a
bottom surface which contacts said substrate; and

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a photocarrier reading element which has a transfer
curve with a first portion for a first part of the light,
that has a first slope, and a second portion for a second
part of the light that has a second slope, where said
second slope is less gradual than said first slope.

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2. A photo sensor as in claim 1 wherein said
photocarrier reading element includes a floating
diffusion, wherein said floating diffusion fills with
charge to produce said first slope, and said photodiode
fills with charge to produce said second slope.

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3. A photosensor as in claim 2 further comprising
a controllable vertical diffusion bridge to control
accumulation exchange in said photodiode.

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4. A photosensor as in claim 3 wherein said
controllable vertical diffusion bridge is formed by a
reset transistor.

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5. A photosensor as in claim 2 further comprising
a second diffusion region, separating said photodiode
from said floating diffusion region.

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6. A photosensor as in claim 5 further comprising
a controlling transistor, controlling whether said first
diffusion region will be coupled to said floating
diffusion region.

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7. A photosensor as in claim 3 wherein said
substrate is a continuous material from said first area
to said bottom area.

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8. A photosensor as in claim 3 further comprising
an output transistor, configured as a follower, and
connected directly to said floating diffusion.

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9. A photosensor comprising:
a semiconductor substrate having an upper surface;

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5 a photodiode, which is fully depleted, is formed of
a first conductivity type material, and is buried below
10 said upper surface to leave a portion of the substrate
over the photodiode and a portion of the substrate below
the photodiode;

15 a floating diffusion region, formed of the same
conductivity type of material as the photodiode, and
coupled to the photodiode; and

20 a reset element, selectively erecting a vertical
diffusion bridge, which when lowered, allows charge in
the photodiode and floating diffusion to spill to and
25 which when raised maintains charge in said floating
diffusion and photodiode.

30 10. A photosensor as in claim 9, wherein said
semiconductor substrate is an opposite conductivity type
35 to said photodiode.

40 11. A photosensor as in claim 9, further comprising
a second diffusion, coupled to said photodiode; and
a transistor separating between said second
45 diffusion and said floating diffusion region, said second
transistor selectively turned on to transfer charge to
said floating diffusion region.

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12. A photosensor as in claim 9 further comprising
a reset diffusion and said reset element is lowered to
transfer charge to said reset diffusion.

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13. A method comprising:

using a buried photodiode to accumulate charge in a
way that produces a transfer characteristic having a
first steeper slope for lower light levels and a second
more gradual slope for higher light levels.

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Prior Art

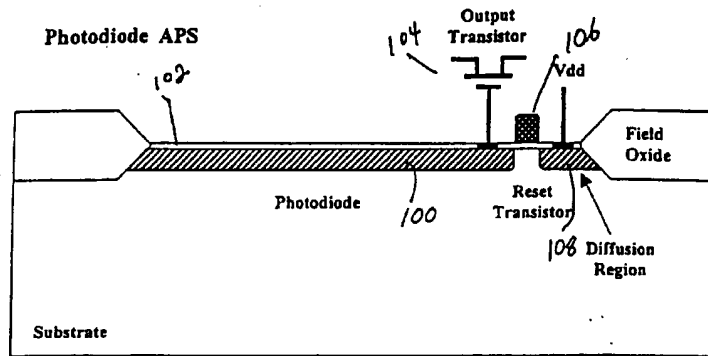


FIG
1A

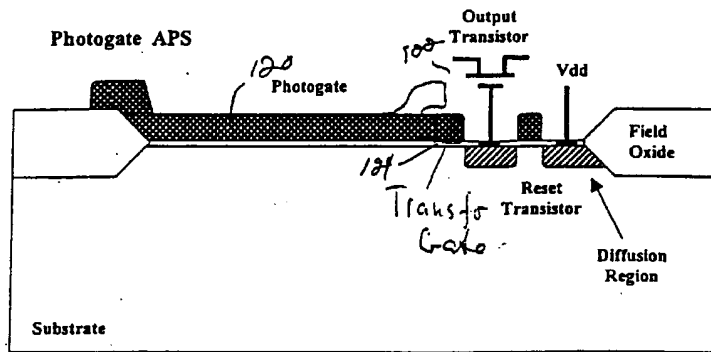


FIG
1B

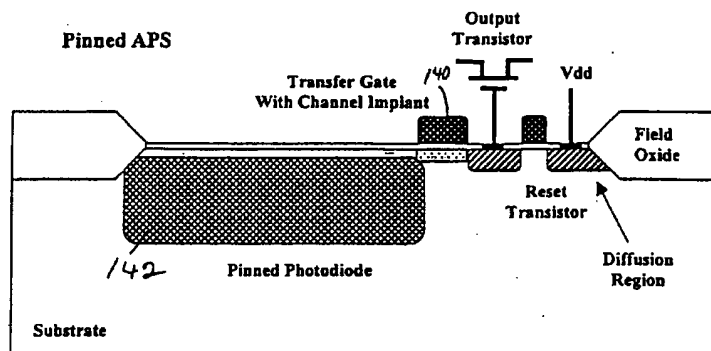
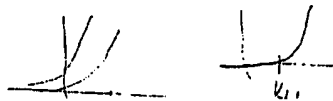


FIG
1C



2/4

Option "A"

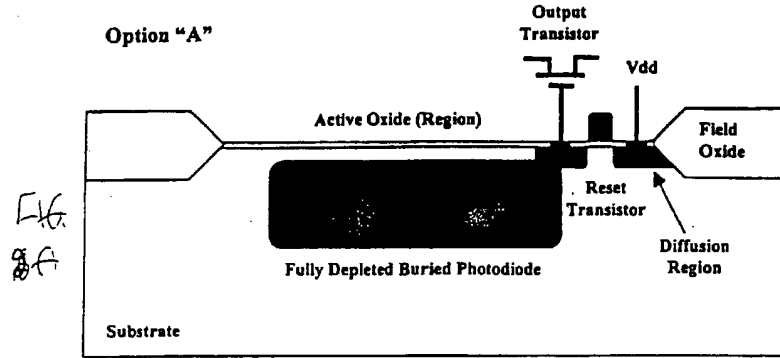


FIG 2A

FIG 2B

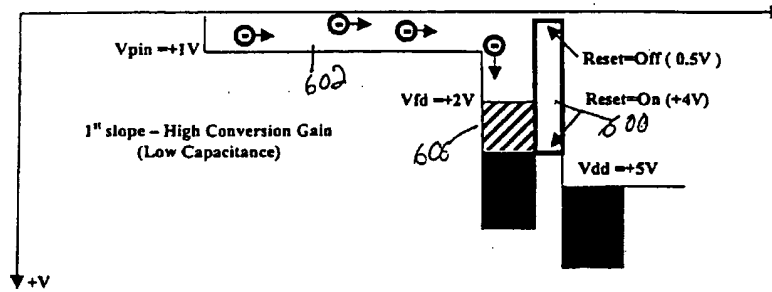


FIG 2C

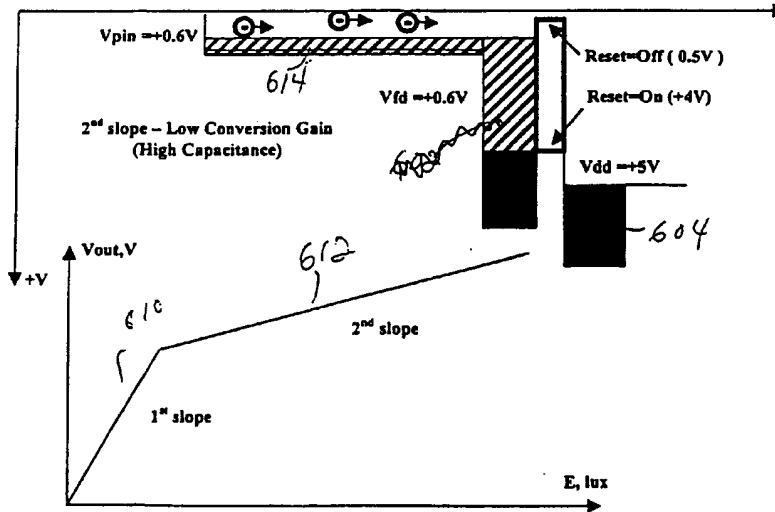
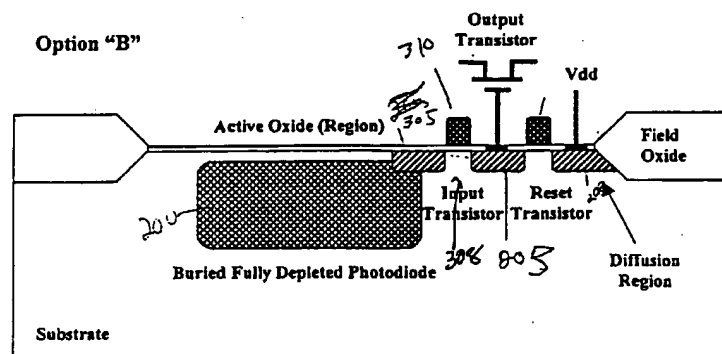


FIG 2D

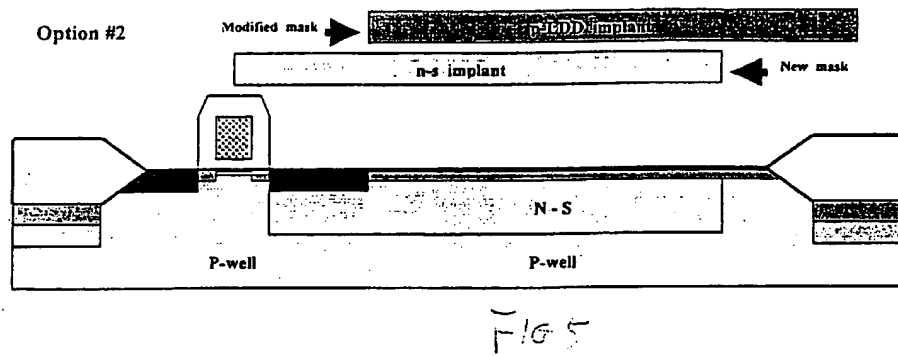
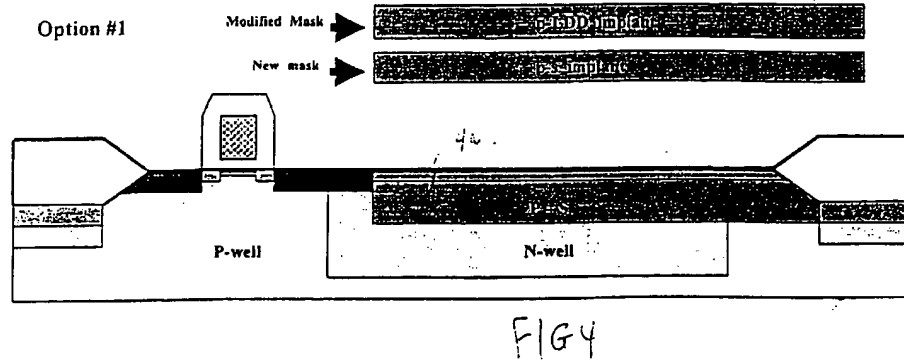
Option "A"

Diagram illustrating a cross-sectional view of a semiconductor device (Option "A"). The device is built on a Substrate (214). A Buried Fully Depleted Photodiode (200) is formed within the substrate. Above the photodiode is a layer of Active Oxide (Region) (210). A Diffusion Region (208) is formed in the substrate, containing an Output Transistor (210) and a Reset Transistor (205). The device is covered by a Field Oxide (202). Other labels include 204, 206, 207, 209, 211, 212, 213, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994,

Fig 2A



F/G 3



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/05545

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 31/06; 31/10
US CL : 250/214.1; 257/292
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 250/214.1; 257/292; 250/208.1. 214R; 257/290, 291, 233, 234, 239

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P	US 5,903,021 A (LEE ET AL) 11 May 1999 (11/05/99), see entire document.	1-13
X	US 5,625,210 A (LEE ET AL) 29 April 1997 (29/04/97), see entire document.	1-13
A	US 5,471,515 A (FOSSUM ET AL) 28 November 1995 (28/11/95), see entire document.	1-13

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"Z" document member of the same patent family

Date of the actual completion of the international search

20 APRIL 2000

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